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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,833	07/24/2001	Tadatoshi Danno	H-997	4278

7590 12/13/2002

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EXAMINER
TOLEDO, FERNANDO L

ART UNIT	PAPER NUMBER
2823	5

DATE MAILED: 12/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/910,833	DANNO ET AL.	
	Examiner	Art Unit	
	Fernando Toledo	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 21-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Claims 19 and 20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 4.

2. Applicant's election without traverse of claims 1 – 18 and 21 – 30 in Paper No. 4 is acknowledged.

Drawings

3. Figures 23 – 28 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1 – 18 and 21 – 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 – 5, 7, 17, 23, 24, 28 – 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Fjelstad (U. S. patent 5,989,939).

In re claim 1, Fjelstad in the U. S. patent 5,989,939; figures 1A – 24 and related text discloses preparing a substrate in which several of electrode members are individually placed on one main surface thereof in separated form (Figure 1A – 1C); placing a semiconductor chip on the one main surface of the substrate and electrically connecting several of electrodes formed on the one main surface of the semiconductor chip and several of electrode members (Figures 3A – 3C); and forming a resin encapsulater for sealing the semiconductor chip and several of electrode members on the one main surface of the substrate (Figures 6 and 7).

In re claim 2, Fjelstad discloses further including a step of separating the semiconductor chip and several of the electrode members from the substrate together with the resin encapsulater (Figure 24).

In re claim 3, Fjelstad discloses wherein the substrate includes a flexible resin film (column 6).

In re claim 4, Fjelstad discloses wherein the substrate includes a flexible resin film having an adhesive layer on one main surface and wherein the semiconductor chip and several of the electrode members are fixed to the substrate by the adhesive layer (Figure 3B).

In re claim 5, Fjelstad discloses wherein the electrodes of the semiconductor chip and the electrode members are electrically connected to one another by bonding wires (Figure 5).

In re claim 7, Fjelstad discloses wherein the substrate is supported by a frame body of a frame structure (Figure 3A).

In re claim 17, Fjelstad discloses preparing a substrate having several of resin encapsulater forming areas on one main surface thereof and having several of electrode members respectively individually placed in the several of resin encapsulater forming areas in separated form (Figure 1A – 1C); placing semiconductor chips on the respective resin encapsulater forming areas of the one main surface of the substrate respectively and respectively electrically connecting several of the electrodes formed on one main surface of each of the semiconductor chip and the several of electrode members within the each resin encapsulater forming area (Figures 3A – 3C); forming a first resin encapsulater for collectively sealing the semiconductor chips and several of

the electrode members placed in the respective resin encapsulater forming areas, on the one main surface of the substrate (Figure 6); dividing the first resin encapsulater every resin encapsulater forming areas to thereby form several of second encapsulaters (Figure 24); separating the semiconductor chips and the several of electrode members from the respective resin encapsulater forming areas of the one main surface of the substrate together with the second resin encapsulater (Figure 24).

In re claim 23, Fjelstad discloses preparing a substrate having a resin encapsulater forming area of one main surface thereof, and several electrode members whose parts of sides are covered with the substrate, and individually placed in the resin encapsulater forming area in separated form; preparing a semiconductor chip with several electrodes formed on the main surface thereof; placing the semiconductor chip on the resin encapsulater forming area of the prepared substrate and respectively electrically connecting several of the electrodes of the semiconductor chip and several of the electrode members; forming a resin encapsulater for sealing the semiconductor chip and several of the electrode members placed in the resin encapsulater forming area, on the one main surface of the substrate; and separating the substrate from the resin encapsulater and several of the electrode members (Figures 1A – 24).

In re claim 24, Fjelstad discloses wherein the electrodes of the semiconductor chip and the electrode members of the substrate are electrically connected to one another by bonding wires (Figure 6).

In re claim 28, Fjelstad discloses preparing a substrate having several resin encapsulater forming areas of one main surface thereof, and several electrode members whose parts of sides are covered with the substrate, and respectively placed

in the resin encapsulater forming areas; preparing several semiconductor chips each having several electrodes formed on the main surface thereof; placing the semiconductor chips on the resin encapsulater forming areas of the prepared substrate and respectively electrically connecting several of the electrodes of each of the semiconductor chip and several of the electrode members of the substrate within each of the resin encapsulater forming area; forming a resin encapsulater for collectively sealing the semiconductor chips and several of the electrode members placed in the respective resin encapsulater forming areas, on the main surface of the substrate; and separating the resin encapsulater between the respective resin encapsulater forming areas; and separating the substrate from the resin encapsulater and several of the electrode members (Figures 1 – 24).

In re claim 29, Fjelstad discloses wherein the electrodes of each of the semiconductor chips and the electrode members of the substrate are electrically connected to one another by bonding wires (Figure 6).

In re claim 30, Fjelstad discloses wherein in the step (e), the resin encapsulater is cut by a dicing method (Figure 24).

8. Claims 8 – 12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicant's Admitted Prior Art (AAPA).

In re claim 8, AAPA discloses preparing a substrate having a nip-holding area and a resin encapsulater forming area surrounded by the nip-holding area both provided on one main surface thereof and having several electrode members individually placed in the resin encapsulater forming area in separated form; placing a semiconductor chip on the resin encapsulater forming area of the one main surface of the substrate and

electrically connecting several of the electrodes formed on the one main surface of the semiconductor chip and several of the electrode members respectively; nipping the nip holding area provided on the one main surface of the substrate by an upper mold and a lower mold of a molding die from upward and downward directions and injecting a resin into a cavity formed between the upper and lower molds of the molding die under pressure in a state in which the resin encapsulater forming area of the one main surface of the substrate, the semiconductor chip and several of the electrode members are placed inside the cavity, thereby forming a resin encapsulater (Figures 23 – 28 of AAPA).

In re claim 9, AAPA discloses further including a step of separating the semiconductor chip and several of the electrode members from the substrate together with the resin encapsulater (Figures 23 – 28).

In re claim 10, AAPA discloses wherein the substrate includes a flexible resin (Figure 23).

In re claim 11, AAPA disclose wherein the substrate includes a flexible resin film having an adhesive layer on one main surface, and wherein the semiconductor chip and several of the electrode members are fixed to the substrate by the adhesive layer (Figure 23).

In re claim 12, AAPA disclose wherein the electrodes of the semiconductor chip and the electrode members are electrically connected to one another by bonding wires (Figure 23).

In re claim 14, AAPA discloses wherein the substrate is supported by a frame body of a frame structure (Figure 23).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando Toledo whose telephone number is 703-305-0567. The examiner can normally be reached on Mon-Fri 8am to 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Fernando Toledo
Examiner
Art Unit 2823

ft
December 5, 2002

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800